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5/0007 (2013.01); **H04W 84/042** (2013.01)(72) Inventors: **Essi Suikkanen**, Oulu (FI); **Johanna**
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The invention relates to an apparatus including: at least one processor and at least one memory including a computer program code, the at least one memory and the computer program code configured to, with the at least one processor, cause the apparatus at least to: choose a modulation, coding and rank scheme; determine a channel quality indicator based on the modulation, coding and rank scheme, and add a detector class indicator to the channel quality indicator for informing capability to a high order modulation if the high order modulation is chosen. In one particular embodiment the high order modulation is 64-QAM and excludes QPSK and 16-QAM, and the added detector class indicator can be a single bit.

